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PATENT
8013-1147

IN THE U.S. PATENT AND TRADEMARK OFFICE

In re application of

Hirokazu HONDA

Conf. 7187

Application No. 09/678,609

Group 2822

Filed October 4, 2000

Examiner David Graybill

MULTILAYER INTERCONNECTION BOARD, SEMICONDUCTOR
DEVICE HAVING THE SAME, AND METHOD OF FORMING THE
SAME AS WELL AS METHOD OF MOUNTING THE SEMICONDUCTOR
CHIP ON THE INTERCONNECTION BOARD

INFORMATION DISCLOSURE STATEMENT

MS ISSUE FEE

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In compliance with Rules 1.97 and 1.98, and in fulfillment of the duty of disclosure under Rule 1.56, the accompanying documents, copies of which are attached to this statement, are made of record on the enclosed Form PTO-1449.

A concise explanation of the relevance of these items is that these references were cited by the Japanese Patent Office in the corresponding Japanese Application Serial No. 2000-57767, filed March 2, 2000. A copy of the Japanese Official Action in which they were cited is attached hereto, with what is believed to be the pertinent portion enclosed in a wavy line. **An English translation of the enclosed portion is also attached hereto.**

Under the provisions of 37 CFR 1.97(e), the undersigned hereby certifies that each item of information

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contained in this Information Disclosure Statement was first cited in any communication from a foreign Patent Office in a counterpart foreign application not more than three months prior to the filing of this Statement.

Charge the \$ 1.17(p) fee of \$180 to Deposit Account No. 25-0120.

Respectfully submitted,

YOUNG & THOMPSON

A handwritten signature in black ink, appearing to read 'Robert J. Patch', written over a horizontal line.

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RJP/fb

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